CLAIMS

What is claimed is:

1. A memory module comprising,

a plurality of memory circuits, wherein at least one of the memory circuits comprises a serial presence detect (SPD) memory circuit;

a plurality of data lines that transfer the data to and from the plurality of memory circuits; and

testing logic coupled to at least one of the plurality of data lines, wherein the testing logic utilizes data stored in the SPD memory circuit to inject a memory error into one or more of the plurality of data lines.

2. The memory module of claim 1 wherein the testing logic, the memory module, and the SPD memory circuit are coupled to a communications bus.

3. The memory module of claim 1 wherein the testing logic applies a bias voltage on at least one of the plurality of data lines based on a request from a software application.

4. The memory module of claim 1 wherein the testing logic further comprises a bus controller that transfers data from the SPD memory circuit.

5. The memory module of claim 3 wherein the testing logic initializes and maintains a counter of the number of data lines to electrically bias.

6. The memory module of claim 1 wherein the testing logic utilizes a column access strobe (CAS) latency stored in the SPD memory circuit to inject a memory error into one or more of the plurality of data lines.

7. The memory module of claim 1 wherein the testing logic utilizes a memory rank stored in the SPD memory circuit to inject a memory error into one or more of the plurality of data lines.

8. A method comprising:

receiving a request to inject an error into a data line of a memory module; and

injecting the error into the data line by a testing logic integrated with the memory module.

9. The method of claim 8 further comprising sending instructions to inject the error to the testing logic from a program executing external to the memory module.

10. The method of claim 9 further comprising sending the instructions on a communication bus.

11. The method of claim 10 further comprising sending the instructions on a serial communications bus.

12. The method of claim 11 wherein the serial communications bus comprises an inter-integrated circuits (I^2C) communications bus.

13. The method of claim 8 further comprises injecting the error into a plurality of data lines.

14. The method of claim 8 further comprising injecting a continuous error into the data line.

15. The method of claim 8 further comprising injecting an error lasting only one memory cycle.

16. A computer readable media storing instructions executable by a computer system to implement a method comprising:

receiving data from a serial presence detect (SPD) memory device;

generating an error injection procedure based in part on the received data; and

applying a bias voltage on at least one data line associated with the error injection procedure.

17. The computer readable media of claim 16 wherein the error injection procedure is generated in response to a request from a software application.

18. The computer readable media of claim 16 wherein the data from the SPD memory device comprises a column access strobe (CAS) latency.

19. The computer readable media of claim 16 wherein the data from the SPD memory device comprises a rank of a memory device.

20. The computer readable media of claim 16 wherein data from the SPD memory device is transported through an inter-integrated circuits (I^2C) communications bus.

21. A system comprising:

a plurality of means for storing data, wherein at least one of the means for storing comprises a serial presence detect (SPD) memory circuit;

a plurality of means for transferring data to and from the plurality of means for storing data; and

a means for applying a bias voltage coupled to the plurality of means for storing data, wherein the means for applying a bias voltage utilizes data stored in the SPD memory circuit to inject an error into at least one of the plurality of means for transferring data.

22. The system of claim 21 wherein the plurality of means for storing data, the SPD memory circuit, and the means for applying a bias voltage are coupled to a communications bus.

23. The system of claim 21 wherein the means for applying a bias voltage electrically biases at least one of the plurality of means for transferring data based on a request from a software application.

24. The system of claim 21 wherein the means for applying a bias voltage further comprises a means for interfacing with a communications bus that is coupled to the SPD memory circuit.

25. The system of claim 21 wherein the means for applying a bias voltage initializes and maintains a counter of the number of the means for transferring data that are to be electrically biased.

26. The system of claim 21 wherein the means for applying a bias voltage biases voltage utilizes a column access strobe (CAS) latency stored in the SPD memory circuit.

27. The system of claim 22 wherein the means for applying a bias voltage utilizes a memory rank stored in the SPD memory circuit.